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A Power Efficient, High Gain R-2R Ladder DAC Designed in 90nm CMOS Technology

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Abstract—*In modern wireless communication system there is a need of broad band transmission of image, audio or video at high data rate, requiring high speed data converters for transmission. In this work an 8 bit Digital to Analog Converter (DAC) is designed, simulated and compared with other available DACs. The designed DAC has very less power consumption of 21.2 mWatt along with DNL and INL of 0.40 and 0.78, Respectively.*

1. INTRODUCTION

In this technological era, electronic industries are moving towards digital edge and most of the signals are generally analog in nature. All aspects like time, speed, weight, accuracy etc. are measured in analog domain, therefore there is a need of data converter. The data converter play most important role in digital signal processing (DSP), it makes a bridge between analog and digital world. The electronic circuits that convert the digital bit to analog signal are called digital to analog converter (DAC), and the electronic circuits that convert an analog signal into digital domain are known as analog to digital converter (ADC) [1]. These converters are essentially useful in DSP, they improves the important features of system like accuracy, linearity, reliability, speed, power and area.

The high speed data converters are designed using different technologies such as GaAs or SiGe [1]. These technologies have drawbacks related to the manufacturing process, power consumption and they are not fabricated on single chip. These limitations are overcome using CMOS technology with low supply voltage. Hence, high speed DACs are integrated with DSP circuitry based on system on a chip (SOC) principle in order to reduce cost.

The dynamic characteristics of DAC such as spurious free dynamic range (SFDR), signal to noise ratio (SNR) including distortion and their static characteristics such as differential non linearity (DNL) and integral non linearity (INL) are important in DSP systems. In this paper section II describes the simple architecture and design pf DAC, section III represents simulation results of the following designs and finally conclusion is written in section IV.

2. ARCHITECTURE OF DAC

Several architectures of high speed DACs are available in the present time such as binary weighted, voltage mode, current mode R-2R ladder type architecture. For appropriate architecture following requirements such as high speed, accuracy, bandwidth, power consumption must be considered. The designing of high bandwidth or high resolution DAC are complex and different types of errors occur, namely gain error, missing code error, absolute error etc., in such a scenario, best performance is given by an 8 bit converter. Simple architecture of a DAC is shown in Fig. [1].

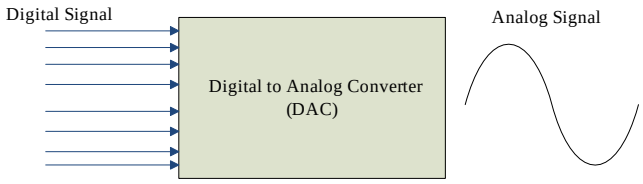

Fig. 1: Block diagram of digital to analog converter

2.1 R-2R Ladder DAC (Without Op-amp)

Sample A voltage mode R-2R ladder type DAC is shown in Fig. [2].

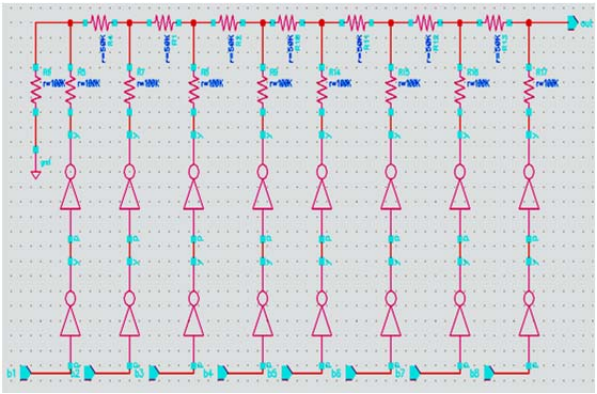

Fig. 2: Schematic of R-2R Ladder type DAC

In this DAC the input impedance varies but output impedance is constant equal to 'R' of R-2R ladder [8].

2.2 R-2R Ladder Op-amp Based DAC

This is the DAC, designed on the basis of Op-Amp based ladder type summing amplifier, shown in Fig. [3].

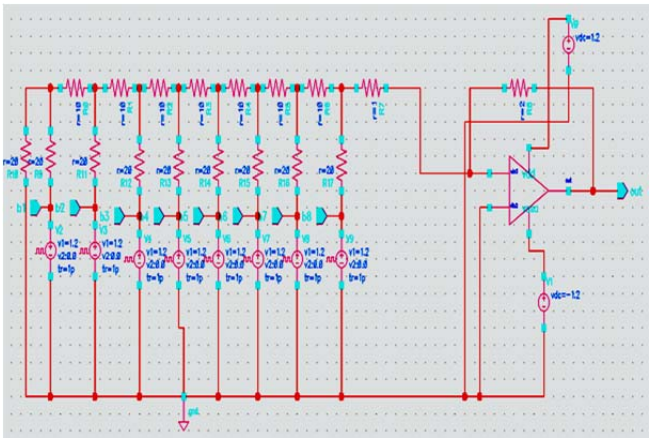

Fig. 3: Schematic of Op-amp Based DAC

3. DESIGNING OF OP-AMP

The op-amp is designed in 90nm CMOS technology for DAC implementation. The op-amp is designed with low supply voltage and less power consumption, shown in Fig. [4].

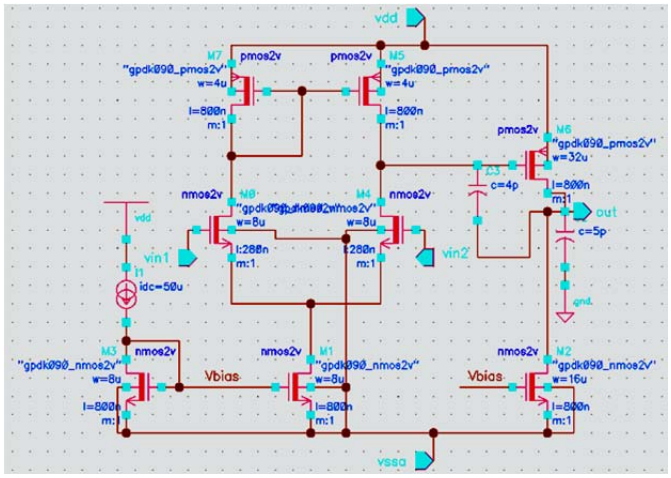

Fig. 4: Schematic of Proposed Op-amp for DAC

CMOS Operational amplifier is most important building block in analog circuit design. This comprises of two stages, first one is differential amplifier and second one is common source amplifier shown in Fig. above. But the additional stage i.e. second stage added a pole in right side of *jw* axis which makes system unstable. There are many techniques that make system stable such as Miller compensation technique, Dominant pole compensation technique and enhance phase compensation technique. In this paper, Miller compensation technique has been used to improve the gain and phase margin. In above Fig. [4], first stage provides a high CMRR, PSRR, low offset, high input impedance and high gain with low noise. The second stage is used for level shifting, adding gain and also behaves as a differential to single ended converter. Designing steps for two stage op-amp are given below for certain specifications:

Step 1: Choose the value of load capacitor C_l and it must lie between 1pF to 4pF and slew rate find from bias current flow in M1.

$$C_c >= 0.22C_l$$

Step 2: Determine the value of current flow in M1 transistor.

$$SR = I/C_c$$

$$I = C_c \times SR$$

Step 3: Design the transistor M0 and M4 using current equations.

$$(W/L)_{1,2} = g_{m0}^2/u_n c_{ox} 2I_{D1}$$

Step 4: Design the transistor M5 and M7 choosing value of input common mode range.

$$(W/L)_{5,7} = \frac{2I_{D3}}{u_p c_{ox}\left[V_{DD} - (ICMR+) - V_{t\max} + V_{t\min}\right]^2}$$

Step 5: Design transistor M1 from calculated value of V_{Dsat}

$$V_{Dsat} >= ICMR(-) - (2I_{D1}/ß_1) - V_{tmax}$$

Using the calculated value of V_{Dsat} design the M1,

$$(W/L)_1 = \frac{2I}{u_n c_{ox}\left(V_{Dsat}\right)^2}$$

Step 6: Design transistor M6 by calculating gm6 and gm5.

$$g_{m6} \geq 10 g_{m0}$$

$$g_{m5} = \sqrt{u_p c_{ox}}\,(W/L).2I$$

$$(W/L)_6 = \frac{g_{m6}}{g_{m5}}(W/L)_5$$

Step 7: Design transistor M2, first calculate the I_6,

$$I_6 = I_2$$

$$\frac{I_6}{I_5} = \frac{(W/L)_6}{(W/L)_5}$$

$$\frac{I_2}{I_1} = \frac{(W/L)_2}{(W/L)_1}$$

First stage gain= $\frac{g_{m5}}{g_{ds4} + g_{ds5}}$

Second stage gain= $\frac{g_{m6}}{g_{ds2} + g_{ds6}}$

Design specification described which are important to get desired response of op-amp, shown in table 1. To get the maximum gain along with minimum power dissipation and good phase margin some changes are required in the feature sizing of transistor, sizing also matters becouse every transistor width increases it size which makes the transistor bulky and take more area, transistor feature sizing shown in table 2.

Table 1: Specifications for designing of two stage op-amp

S.No.	Parameters	Value
1.	V_{DD}	1.2
2.	ICMR(+)	0.8
3.	ICMR(-)	0.5
4.	Gain bandwidth product	20MHz
5.	Open loop gain	60db
6.	Phase margin	60
7.	Slew rate	20v/us
8.	Load capacitance	5pf

Table 2: Effect on gain and power dissipation by varying feature size

I_{DC}	$W_{0,4}$	$W_{5,7}$	$W_{1,3}$	W_6	W_2	Gain(db)	Power dissipation
30u	15u	20u	10u	20u	15u	23.63	62.18u
30u	15u	20u	10u	25u	13u	31.4	67.67u
30u	15u	30u	25u	25u	13u	45.93	56.52u
30u	15u	25u	25u	25u	25u	46.03	58.47u

4. SIMULATION RESULTS

After simulations the output waveforms of two stage op-amp and DAC based on op-amp shown in figures below.

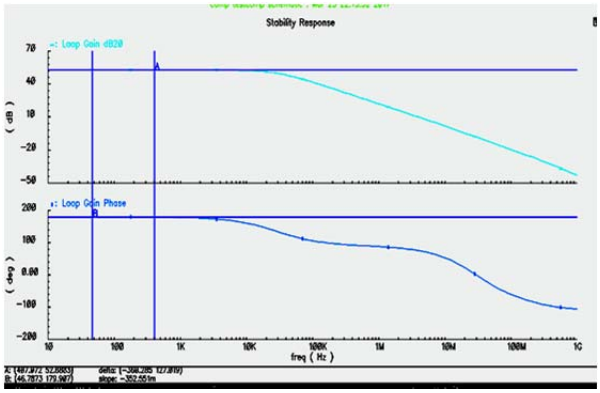

Fig. 7: Op-amp gain and phase plot

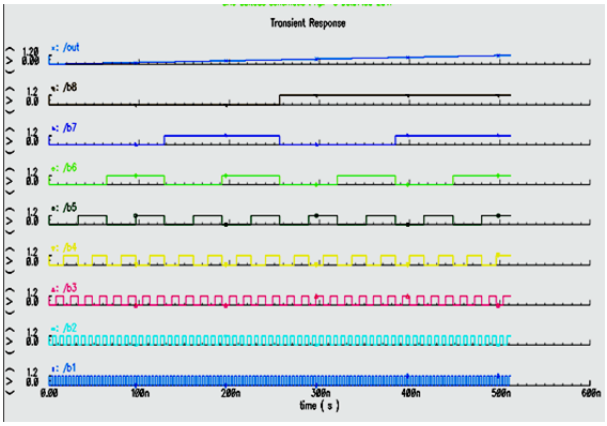

Fig. 8: Output of op-amp based DAC

Table 1: Comparative study on DAC Power dissipation among different research paper.

Specification (Unit)	[2]	[3]	[4]	This Work
Supply Voltage (Volt)	1.2	1.2	1	1.2
Resolution (Bit)	10	12	10	8
Process (nm)	90	90	90	90
Power Consumption (mW)	23	128	49	21.2
DNL	-	0.5	-	0.40
INL	-	1.2	-	0.78

5. CONCLUSION

The 8 bit R-2R Ladder DAC using Op-Amp is designed and simulated in 90 nm CMOS Technology. As Op-Amp is a active device, so this DAC can be used to convert very weak digital signals to amplified Analog signals. Along with this, as the design is carried out in 90 nm CMOS technology, provides sufficient power saving and full output swing. DNL and INL performance of the designed DAC is also good as compared to previously designed DACs.

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